ABSTRACT OF THE DISCLOSURE

A clock/data recovery circuit used in a receiving apparatus is provided in the circuit including: a voltage control oscillator for generating a clock signal of a frequency of 1/K of a bit rate of an input data signal; a delay circuit; a demultiplexer for demultiplexing the input data signal; a multiplexer for multiplexing the demultiplexed signals; a phase comparator for comparing phases of an output signal of the delay circuit and an output signal of the multiplexer; a lowpass filter; wherein the clock/data recovery circuit outputs the clock signal generated by the voltage control oscillator as a recovery divided clock signal, and outputs the demultiplexed signals output as recovery parallel data signals.